Abstracts

HiperLAN 5.4-GHz low-power CMOS synchronous oscillator (Sep. 2001 [T-MTT])

Y. Deval, J. Begueret, A. Spataro, P. Fouillat, D. Belot and F. Badets. "HiperLAN 5.4-GHz low-power CMOS synchronous oscillator (Sep. 2001 [T-MTT])." 2001 Transactions on Microwave Theory and Techniques 49.9 (Sep. 2001 [T-MTT] (Mini-Special Issue on the 2001 IEEE Radio Frequency Integrated Circuit (RFIC) Symposium)): 1525-1530.

A 5.4-GHz 0.25-/spl mu/m very-large-scale-integration CMOS synchronous oscillator (SO) is proposed in this paper, which is designed to act as a local oscillator for HiperLAN systems. The advantage of using such an oscillator in a double-loop frequency synthesizer is demonstrated. The design strategy leading to an optimized SO with regards to its synchronization range is described. A test chip is presented, which provides a 150-MHz synchronization range and a -97-dBc/Hz phase noise at 10-kHz offset from the 5-GHz carrier, while consuming only 5 mA from a 2.5-V supply.

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